UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,092	06/28/2002	Gilbert Wolrich	10559-309US1	7323

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EXAMINER
RIZZUTO, KEVIN P

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
Office Action Summary		10/070,092	WOLRICH ET AL.
		Examiner	Art Unit
		Kevin P Rizzuto	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>05 January 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12-19 and 21-27* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-10, 12-19, 21-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1, 3-10, 12-19 and 21-27 have been examined.

2.   Acknowledgement of papers filed: amendment filed on 1/5/06. The papers filed

have been placed on record.

Withdrawn Claim Objections/Rejections

3.   Applicant, via amendment, has overcome the 35 U.S.C. 103 Rejections to claim

1-27 set forth in the previous Office Action. Consequently, the examiner has withdrawn

these rejections.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1, 3, 5, 7 and 8 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Byers et al., U.S. Patent 5,487,159, herein referred to as Byers,

in view of Hennessy and Patterson, Computer Organization and Design and

further in view of Hennessy and Patterson, Computer Architecture, A Quantitative

Approach.

6.   As per claim 1, teaches a hardware-based multithreaded processor comprising a

plurality of microengines, each of the microengines comprising:

        -A control store: [Control Store 10, fig. 1]

        -Controller logic: [Command Decode 14, fig. 1]

        -And an execution box data path [data path hardware shown in fig. 1] including

an arithmetic logic unit [ALU 34] and a general purpose register set [Local Store 16] the

execution box performing functions in response to instructions: [Fig. 1]

        -One of the instructions causing the execution box to selectively load any

specified combination of bytes of data within a transfer register associated with one

microengine, with a shifted value of an operand that preserves the bytes of data that are

not loaded: [The Shift, mask and merge instruction has a source and destination field for

specifying the source and destination registers. This allows the source and destination

registers to be the same register, as is well known in the art. When the source and

destination specify the same general register in Local Store 16, and R = 1, the BUSR

register data is shifted, masked and merged with the source register (REG A). (See fig.

4). The Mask/Merge Register 24 holds the mask and merge bits which selectively load

any specified combination of bytes of data within the transfer register (destination

register) with a shifted value (shifted BUSR data) and the bytes of data that are not

loaded (not overwritten by shifted BUSR data) are preserved in REG A (transfer

register) because the source register is the same as the destination register. The

general explanation of the execution box data path including register access is on col. 4,

lines 26-67. The explanation of the shift, mask and merge instruction is in col. 5, lines

6-53. Fig. 4 is a flow chart for the shift, mask and merge instruction and is described on col. 6, lines 15-34. Figs. 3-10 and col. 6, line 36 to col. 7, line 44 illustrate an exemplary shift, mask and merge instruction.]

-With loading using an associated bit mask with each bit of the associated bit mask identifying a different byte of the transfer register: [The transfer register is made up of 36 bits, or 4 ½ bytes. Each of the four full bytes has a corresponding four full bytes of corresponding mask/merge bits in the mask/merge register 24. The associated "bit mask" is made up of each of the mask bits 0 shown in fig. 3. Each mask bit 0 identifies the corresponding bits 1-0 within the transfer register (REG A) and since each of the corresponding bits 1-0 is part of a different byte of the transfer register, each mask bit 0 of the mask/merge bit register 24 identifies a different byte of the transfer register. Col. 5, lines 36-53.]

7.   While Byers teaches a transfer register associated with one microengine, Byers fails to teach that the microengine is one of a plurality of microengines or that the microengines contain context event switching logic.

8.   Hennessy and Patterson teach that it is beneficial to connect multiple microengines together to become a multiprocessor (page 712 of Computer Organization and Design). Duplicating the microengine taught by Byers and using them together as a multiprocessor system as taught in Hennessy and Patterson would cause the microengine of Byers to be one of a plurality of microengines. The multiprocessor system provides increased processing speeds and capabilities, which would have

provided the motivation to one of ordinary skill in the art to combine the teachings of

Byers with Hennessy and Patterson (Page 712).

9.   Byers, in view of Hennessy and Patterson, Computer Organization and Design,

fails to teach context switching logic.

10.   Hennessy and Patterson, A Quantitative Approach, teach that context switching

logic allows a processor to run multiple processes at once (i.e., time sharing). Time-

sharing the processor among multiple users/processes causes a single processor to

create the illusion that all users have their own machine. (Pages 447-449)

11.   It would have been obvious to one of ordinary skill in the art to add context

switching logic to the microengines taught in Byers, in view of Hennessy and Patterson,

Computer Organization and Design, as taught in Hennessy and Patterson, A

Quantitative Approach. Causing a single processor to create the illusion of multiple

processors, which allows multiple users to simultaneously each have their own process

running on the single processor, would have provided the motivation to one of ordinary

skill.

12.   Furthermore, while Byers teaches in the first embodiment, that each mask bit in

the mask/merge register 24 corresponds to two bits in the transfer register, which has

been shown to apply to the instant claims, Byers also suggests altering the number of

bits the mask bit corresponds. Byers teaches that the more mask bits in the

mask/merge register 24, the more flexibility allowed while masking and merging.

However, Byers also teaches that the more mask bits, the larger the mask/merge

register needs to be, thus an undesired increase in space is required. (Col. 5, lines 34-

67) In light of the teachings of Byers, one of ordinary skill in the art would have recognized to reduce the number of mask/merge bits to a number wherein each mask/merge bit corresponds to a single byte, thus reducing the amount of space required to store the mask/merge bits.

13.   As per claims 3, Byers, in view of Hennessy and Patterson, teaches wherein the instruction further comprises a field that indicates a left shift n bits, where n is a number from one to thirty-one (Col. 5, lines 23-36 and fig. 3).

14.   As per claims 5, Byers, in view of Hennessy and Patterson, teaches wherein the instruction further comprises a field that indicates a right shift n bits, where n is a number from one to thirty-one. (Col. 5, lines 23-36 and fig. 3).

15.   As per claims 7, Byers, in view of Hennessy and Patterson, teaches wherein the instruction further comprises a field that indicates a left rotate n bits, where n is a number from one to thirty-one. (Col. 5, lines 23-36 and fig. 3, furthermore, figs. 8 shows non-rotated data and fig. 9 shows the data rotated left 3 bits.)

16.   As per claims 8, Byers, in view of Hennessy and Patterson, teaches wherein the instruction further comprises a field that indicates a right rotate n bits, where n is a number from one to thirty-one. (Col. 5, lines 23-36 and fig. 3, furthermore, figs. 8 shows non-rotated data and fig. 9 shows the data rotated left 3 bits. By altering the L bit of the instruction, a left/right adjustment is made.)

17.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Byers et al., U.S. Patent 6,487,159, herein referred to as Byers, in view of Hennessy and Patterson, Computer Organization and Design, in view of Hennessy and

Patterson, Computer Architecture, A Quantitative Approach and further in view of

Hao, U.S. Patent 4,569,016.

18.   As per claims 4, Byers fails to teach wherein the instruction further comprises a

field that indicates a left shift by an amount specified in five bits of the operand of a

previous instruction, where the lower five bits is a number from one to thirty-one.

19.   However, Hao teaches, RMI and RNM instructions (shift, mask and merge

instructions), wherein the shift amount is indicated by an amount specified in 5 bits (bits

27-31) of the RB register. It is inherent that in order for data to be in the RB register to

specify a shift amount, it must have been an operand of a previous instruction (Column

13, lines 29-42 and lines 55-70 and Column 25, lines 56-66))

20.   It would have been obvious to indicate the shift amount via a register since this

allows a larger number of shift amounts to be specified. Byers only teaches 4 bits

specifying the shift amount, which can only encode 16 different shift amounts.

However, using the 4 bits to specify a register, as is taught in Hao, would allow the

register to specify the shift amount, which would enable the shift amount range to

increase. Therefore, it would have been obvious to one of ordinary skill in the art to

specify the shift amount using a register such as taught in Hao.

21.   Furthermore, Examiner takes Official Notice that using register operand data

instead of immediate operand data is well known in the art. Altering the system of

Byers to use a register operand to specify the shift amount would have been obvious to

one of ordinary skill in the art since Examiner takes Official Notice that using register

operand data in place of immediate operand data is well known in the art.

22.   While Byers, in view of Hao and/or the Official Notice, teaches that the shift

amount is specified in 5 bits of a first operand of a previous instruction, it is not taught

that the 5 bits are in a lower five bits of the operand.

23.   It would have been obvious to one of ordinary skill in the art at the time the

invention was made to place the 5 bits that specify the shift amount into the lower 5 bits

of register RB instead of the upper 5 bits since one of ordinary skill in the art would have

recognized that the mere rearrangement of parts that does not modify the operation of

the device does not make said device patentable.

24.   As per claims 6, Byers fails to further teach wherein the instruction further

comprises a field that indicates a right shift by an amount specified in a lower five bits of

the first operand of a previous instruction, where the lower five bits is a number from

one to thirty-one.

25.   However, Hao teaches, RMI and RNM instructions (shift, mask and merge

instructions), wherein the shift amount is indicated by an amount specified in 5 bits (bits

27-31) of the RB register. It is inherent that in order for data to be in the RB register to

specify a shift amount, it must have been an operand of a previous instruction (Column

13, lines 29-42 and lines 55-70 and Column 25, lines 56-66))

26.   It would have been obvious to indicate the shift amount via a register since this

allows a larger number of shift amounts to be specified. Byers only teaches 4 bits

specifying the shift amount, which can only encode 16 different shift amounts.

However, using the 4 bits to specify a register, as is taught in Hao, would allow the

register to specify the shift amount, which would enable the shift amount range to

increase. Therefore, it would have been obvious to one of ordinary skill in the art to specify the shift amount using a register such as taught in Hao.

27.   Furthermore, Examiner takes Official Notice that using register operand data instead of immediate operand data is well known in the art. Altering the system of Byers to use a register operand to specify the shift amount would have been obvious to one of ordinary skill in the art since Examiner takes Official Notice that using register operand data in place of immediate operand data is well known in the art.

28.   While Byers, in view of Hao and/or the Official Notice, teaches that the shift amount is specified in 5 bits of a first operand of a previous instruction, it is not taught that the 5 bits are in a lower five bits of the operand.

29.   It would have been obvious to one of ordinary skill in the art at the time the invention was made to place the 5 bits that specify the shift amount into the lower 5 bits of register RB instead of the upper 5 bits since one of ordinary skill in the art would have recognized that the mere rearrangement of parts that does not modify the operation of the device, does not make said device patentable.

30.   **Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Byers et al., U.S. Patent 6,487,159, herein referred to as Byers, in view of Hennessy and Patterson, Computer Organization and Design, in view of Hennessy and Patterson, Computer Architecture, A Quantitative Approach, in view of Hao, U.S. Patent 4,569,016 and further in view of Kiuchi, U.S. Patent 5,832,258.**

31.   As per claim 9, Byers, in view of Hennessy and Patterson, teach the processor of claim 1.

32.   However, Byers fails to further teach, wherein the instruction further comprises

an optional token that is set by a programmer and specifies to set arithmetic logic (ALU)

condition codes based on a result formed in the ALU.

33.   Kiuchi teaches the optional updating of a condition register depending on an

optional token (CC field) encoded in an instruction. When the CC field is set to 0001, an

unconditional instruction does not update the condition codes in a condition register

(Column 37, lines 59-62). The Condition Code decoder is explained in columns 31 and

32, the CC codes and their meanings are taught in Table 1, Columns 37 and 38. This

provides the benefit of greater program flexibility and a reduction in code size ("Objects

of the invention", Column 2 and "Advantages of Conditional Data Operation with No

Condition Code Update," Columns 51 and 52). It would have been obvious to one of

ordinary skill in the art to combine the invention of Kiuchi with the invention of Hao in

view of Hennessy and Patterson because of the benefits Kiuchi teaches.

34.   Claims 10, 12, 14, 16, 17, 19, 21, 23, 25 and 26 are rejected under 35 U.S.C.

103(a) as being unpatentable over Byers et al., U.S. Patent 5,487,159, herein

referred to as Byers, in view of Hennessy and Patterson, Computer Organization

and Design.

35.   As per claim 10, given the similarities between claim 1 and claim 10, the

arguments as stated for the rejection of claim 1 also apply to claim 10. The additional

limitation, "clearing the bytes of data that are not loaded" which is used in place of

preserving the bytes of data that are not loaded from claim 1, is taught by Byers. The

Merge and Mask bits can be set appropriately so as to clear the bytes of data that are

not loaded. If the mask bit is set to 0, and the merge bit is set to 0, the bytes of data of

the transfer register (REG A) that are not loaded with Bus Register 20 (because the

associated merge bits are set to 0) are cleared.

36.   As per claim 19, given the similarities between claim 1 and claim 19, the

arguments as stated for the rejection of claim 1 also apply to claim 19.

37.   Given the similarities between claim 3 and claims 12 and 21, the arguments as

stated for the rejection of claim 3 also apply to claims 12 and 21.

38.   Given the similarities between claim 5 and claims 14 and 23, the arguments as

stated for the rejection of claim 8 also apply to claims 14 and 23.

39.   Given the similarities between claim 7 and claims 16 and 25, the arguments as

stated for the rejection of claim 7 also apply to claims 16 and 25.

40.   Given the similarities between claim 8 and claims 17 and 26, the arguments as

stated for the rejection of claim 8 also apply to claims 17 and 26.

41.   **Claims 13, 15, 22 and 24 are rejected under 35 U.S.C. 103(a) as being**

unpatentable over Byers et al., U.S. Patent 6,487,159, herein referred to as Byers,

in view of Hennessy and Patterson, Computer Organization and Design and

further in view of Hao, U.S. Patent 4,569,016.

42.   Given the similarities between claim 4 and claims 13 and 22, the arguments as

stated for the rejection of claim 4 also apply to claims 13 and 22.

43.   Given the similarities between claim 6 and claims 15 and 24, the arguments as

stated for the rejection of claim 6 also apply to claims 15 and 24.

44.   **Claims 18 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable**

over Byers et al., U.S. Patent 6,487,159, herein referred to as Byers, in view of

Hennessy and Patterson, Computer Organization and Design, in view of Hao, U.S.

Patent 4,569,016 and further in view of Kiuchi, U.S. Patent 5,832,258.

45.   Given the similarities between claim 9 and claims 18 and 27, the arguments as

stated for the rejection of claim 4 also apply to claims 18 and 27.

Response to Arguments

46.   Applicant's arguments filed on 1/13/2006 have been fully considered but those

involving Hao, U.S. Patent 4,569,016 are found moot in view of the new rejections

above.

47.   Applicant's arguments regarding Kiuchi have been fully considered but are not

found persuasive.

48.   Applicant primarily argues:

> "But nowhere in Kiuchi's Table 1, or elsewhere in Kiuchi, does Kiuchi disclose or suggest an
> instruction that 'comprises an optional token that is set by a programmer and specifies to set
> arithmetic logic unit (ALU) condition codes based on the result formed in the ALU,' as required by
> applicant's claim 9. Further, the condition codes or flags that are set by the ALU after execution
> of instructions that specify examination of condition codes fails to suggest the claimed option
> token, since the optional token is specified by the programmer."

49.   Applicant's arguments are not found persuasive for the reasons given below.

    a.   As Applicant states in the remarks section, "Kiuchi describes instructions

that include <u>condition code fields that</u> identify predefined conditions and also

<u>identify whether a condition code register should be updated when the data</u>

<u>processing operation is performed by the execution unit</u> of a digital signal

processor (Abstract)." [Remarks, page4, lines 3-5]. Therefore, Kiuchi has

taught, "an optional token that... specifies to set arithmetic logic unit (ALU)

condition codes based on the result formed in the ALU" as claimed.

Furthermore, Kiuchi teaches that the condition code field is set by a programmer.

In the background, col. 2, lines 6-15, it is taught that a programmer is constrained

by not having the ability to disable condition code register updating. It is also

taught that in the "Objects of the Invention" that the ability to execute instructions

without updating a condition code register in order to allow "greater flexibility and

creativity in developing programs." (Col. 2, lines 23-27) Furthermore, it is stated

on under "Advantages of Conditional Data Operation With No Condition Code

Update" on col. 51, lines 37-50, "Referring to Table 1, the flags generated when

one of the instruction types... is executed are not updated if the condition code

specifies the second non-condition (0001) or one of the 14 conditions (0010-

1111). This provides the advantage of enabling a subsequent instruction to be

conditionally executed based on flags (i.e., conditions) generated or set during

the execution stages of earlier executed unconditional instructions. As a result, if

the programmer of the DSP 1100 desires to make use of a specific condition for

a conditional branch or conditional data operation, then he/she is not restricted to

include such a conditional instruction immediately after the data operation

instruction which resulted in the condition code." It is inherent that a programmer

sets the condition code bits, if a programmer did not set the condition code bits

how he/she desired, the programmer would lack the flexibility that Kiuchi states

the invention gives him or her. The only way for the programmer to take

advantage of the disclosed benefits is if the programmer is able to set the

condition codes appropriately.

Conclusion

50.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a

rejection of claims in an application or patent under reexamination, the applicant or

patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments
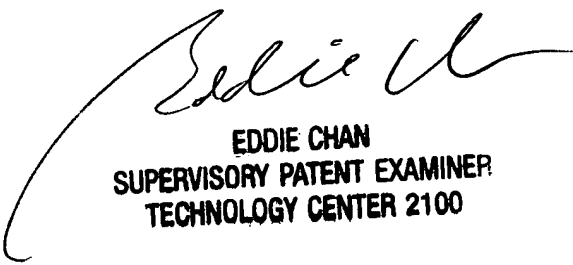
avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-

4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on (571) 272-4174. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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KPR

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TECHNOLOGY CENTER 2100